Design and Implementation of Testable Reversible Sequential Circuits and Garbage Output

Manikandan.B[#1],Vijayaprabhu.A[#2]
M.E. Department of VLSI Design (ECE)[#1], Assistant Professor ECE Dept[#2]
Sri Venkateswara College of Engineering and Technology, Anna University
manicando91@gmail.com[#1], china_durai1@yahoo.co.in[#2]

Abstract— The conservative reversible gates are used to designed reversible sequential circuits. The sequential circuits are flip flops and latches. The conservative logic gates are Feynman, Toffoli, and Fredkin. the design of two vectors testable sequential circuits based on conservative logic gates. All sequential circuit based on conservative logic gates can be tested for classical unidirectional stuck-at faults using only two test vectors. The two test vectors are all 1s, and all 0s. The designs of two vectors testable latches, master-slave flip-flops and double edge triggered (DET) flip-flops are presented. We also showed the application of the proposed approach toward 100% fault coverage for single missing/additional cell defect in the quantum- dot cellular automata (QCA) layout of the Fredkin gate. The conservative logic gates are in terms of complexity, speed and area.

Index Terms— Reversible Logic, Sequential Circuits, Quantum dot Cellular Automata, D-Latch, Barrel Shifter, Flip Flop, Test mode.

1 INTRODUCTION

Conservative logic is called reversible conservative logic when there is a one-to-one mapping between the inputs and the outputs vectors along with the property that there are equal number of 1s in the outputs as in the inputs. Conservative logic circuits are not reversible, if one-to-one mapping between the inputs and the outputs vectors is not preserved.

Conservative logic can be reversible in nature or may not be reversible in nature. Reversibility is the property of circuits in which there is one to- one mapping between the inputs and the output vectors, that is for each input vector there is a unique output vector and vice-versa.

QCA is one of the emerging nanotechnologies in which it is possible to implement reversible logic gates. QCA makes it possible to achieve circuit densities and clock frequencies beyond the limits of existing CMOS technology. In QCA, computing logic states of 1 and 0 are represented by the position of the electrons inside the QCA cell. Thus, when the bit is flipped from 1 to 0 there is no actual discharging of the capacitor as in conventional CMOS. Hence, QCA does not have to dissipate all its signal energy during transition. Further, propagation of the polarization from one cell to another is because of interact -tion of the electrons in adjacent QCA cells. As there is no movement of electrons from one QCA cell to the other, there is no current flow. Therefore, QCA has significant advantage compared to CMOS technology in terms of power dissipation. Due to high error rates in nano-scale manufacturing, QCA and other nanotechnologies target reducing device error rates.

This paper is organized as follows. Section II presents the conservative logic gates, Section III presents design of testable reversible latches, Section IV describes QCA, Section V presents design of testable reversible flip-flop, Section VI discusses the application of the proposed two vectors, all 0s and all 1s, Section VII provides some discussions and conclusions.

2 CONSERVATIVE LOGIC GATES

In order to design the sequential circuits, the conventional logic gates are appropriately designed from the reversible gates. The reversible gates used to design the conventional logic are so chosen to minimize the number of reversible gates used and garbage outputs produced. The design of AND function using Fredkin gate. The design of NAND and NOR function using New Gate respectively. Feynman Gates can be used for copying the outputs and to avoid the fan out problem in reversible logic. In the Feynman gate, there are exactly two outputs corresponding to the inputs and a '0' in the second input will copy the first input to both the outputs of that gate. Hence it can be concluded that Feynman gate is the most suitable gate for single copy of bit since it does not produces any garbage output. The Feynman gate as copying output and NOT function respectively. May stuck at 0 or 1 leading to accessing wrong address, no address, or multiple addresses.

- *Manikandan.B is currently pursuing masters degree program in VLSI Design in Anna University,India, PH-09677640337. E-mail: manicando91@gmail.com*
- *Vijaya Prabhu.A is currently pursuing Asst. Prof in Electronics and CommunicationEngg in Anna University,India, PH-09894453481. E-mail: vijayaprabhu85@gmail.com*

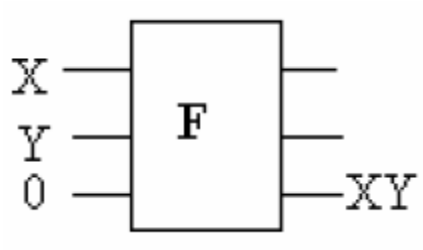

Fig.1 Fredkin Gate as AND Gate

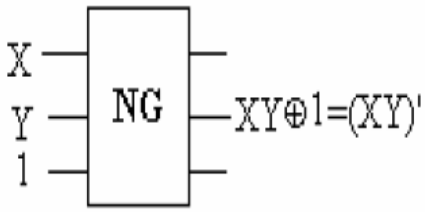

Fig.2 New Gate As NAND Gate

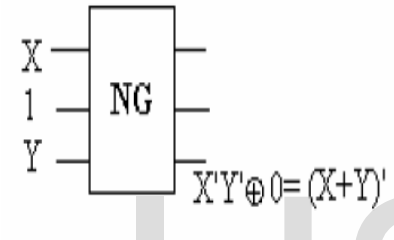

Fig.3 New Gate As NOR Gate

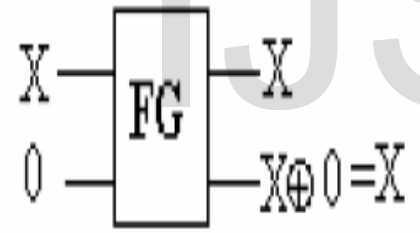

Fig.4 Feynman Gate As Copying Output

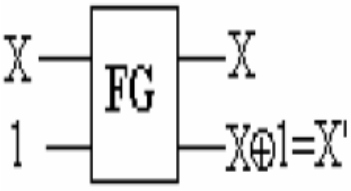

Fig.5 Feynman Gate As Not Gate

Novel Reversible Flip Flops are designed using Feynman Gate, New gate and Fredkin Gate. The designed FFs are highly optimized in terms of number of reversible gates and garbage outputs.

Reversible logic elements, both with and without the property of conservatism, can be defined in many different logic systems. For the purposes of this paper, the class of reversible elements that can be modeled as binary-valued logic circuits will be called classical reversible logic elements. Much work has been done in defining and characterizing classical reversible logic and applying the concepts toward power conservation and specific technology implementations. This section will briefly define basic results in classical reversible logic.

$x^+ = x$ $y^+ = y$ $z^+ = xy \oplus z$	TOF3(x,y,z)
$x^+ = x$ $y^+ = \bar{x}y \oplus xz$ $z^+ = \bar{x}z \oplus xy$	FRE(x,y,z)

Table.1 Gate functionality

2

3

3 DESIGN REVERSIBLE LATCHES

The characteristic equation of the D latch can be written as $Q+ = D \cdot E + .E \cdot Q$. In the proposed work, enable (E) refers to the clock and is used interchangeably in place of clock. When the enable signal (clock) is 1, the value of the input D is reflected at the output that is $Q+ = D$. While, when $E = 0$ the latch maintains its previous state, that is $Q+ = Q$. The reversible Fredkin gate has two of its outputs working as 2:1 MUxes, thus the characteristic equation of the D latch can be mapped to the Fredkin gate (F). The realization of the reversible D latch using the Fredkin gate. But FO is not allowed in conservative reversible logic. Moreover, the design cannot be tested by two input vectors all 0s and all 1s because of feedback, as the output Q would latch 1 when the inputs are toggled from all 1s to all 0s and could be misinterpreted as stuck-at-1 fault.

In this paper, we propose to cascade another Fredkin gate to output Q as shown in Fig. The design has two control signals, C1 and C2. The design can work in two modes: normal mode and test mode.

3.1 NORMAL MODE

The normal mode is shown in Fig. in which we will have $C1C2 = 01$ and we will have the design working as a D latch

without any fan-out problem.

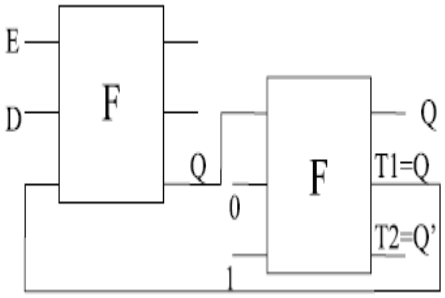

Fig.6 Fredkin gate based D Latch in normal mode: *C*1 = 0 and *C*2 = 1

3.2 TEST MODE

In test mode, when *C*1*C*2 = 00 as shown in Fig. it will make the design testable with all 0s input vectors as output T1 will become 0 resulting in making it testable with all 0s input vectors. Thus, any stuck-at-1 fault can be detected. When *C*1*C*2 = 11 as shown in Fig. the output T1 will become 1 and the design will become testable with all 1s input vectors for any stuck-at-0 fault. It can seen from above that C1 and C2 will disrupt the feedback in test mode, and in normal mode will take care of the fan-out. Thus, our proposed design works as a reversible D latch and can be tested with only two test vectors, all 0s and all 1s, for any stuck-at fault by utilizing the inherent property of conservative reversible logic.

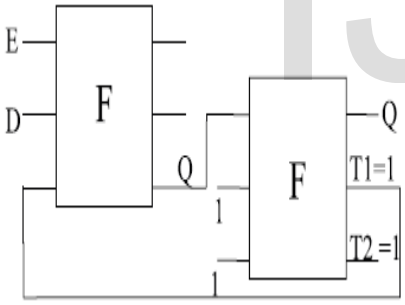

Fig.7 Fredkin gate based D latch in test mode for stuck-at-0 fault: *C*1 = 1 and *C*2 = 1.

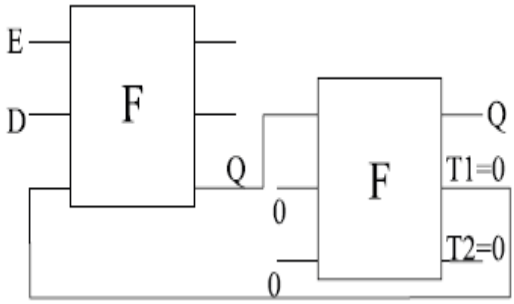

Fig.8 Fredkin gate based D latch in test mode for stuck-at-1 fault: *C*1 = 0 and *C*2 = 0.

4 QUANTUM-DOT CELLULAR AUTOMATA

Quantum-dot cellular automata (QCA) is a nanotechnology that has recently been recognized as one of the top six emerging technologies with potential applications in future computers. Several studies have reported that QCA can be used to design general-purpose computational and memory circuits. First proposed in 1993 by Lent et al., and experimentally verified in 1997, QCA is expected to achieve high device density, extremely low power consumption, and very high switching speed. The fundamental QCA logic primitives are the three-input majority gate, wire, and inverter. Each of these can be considered as a separate QCA locally interconnected structure, where QCA digital architectures are combinations of these cellular automata structures. Traditional logic reduction methods, such as Karnaugh maps (K-maps), always produce simplified expressions in the two standard forms: sum of products (SOP) or product of sums (POS). However, we will encounter difficulties in converting these two forms into majority expressions due to the complexity of multilevel majority gates. In CMOS/silicon design, the logic circuits are usually implemented using AND, OR gates based on SOP or POS formats. However, since QCA logic is based on a majority gate primitive, it is critical that an efficient technique be established for designing with this primitive. In this paper, we develop a Boolean algebra based on a geometrical interpretation of three-variable Boolean functions to facilitate the conversion of sum-of-products expressions into reduced majority logic. Thirteen standard functions are introduced, which represent all possible three-variable Boolean functions. For each of these standard functions, we present the reduced majority expression. As an example of this technique, we present a QCA adder design, and show that the proposed method is able to reduce the total hardware, as compared to previously published designs.

4.1 QCA LOGIC DEVICES

The fundamental QCA logic primitives include a QCA wire, QCA inverter, and QCA majority gate, as described below.

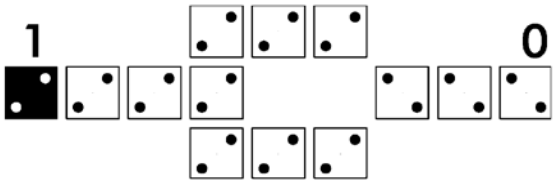

Fig.9 QCA Inverter

4.2 QCA CLOCK

A QCA clock consists of four phases which are called

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Switch, Hold, Release, and Relax as shown in Fig. During the Switch phase, the inter dot barriers are slowly raised and the QCA cells become polarized according to the state of their drivers (that is, their input cells). During the Hold phase, the interdot barriers are kept high and the QCA cells

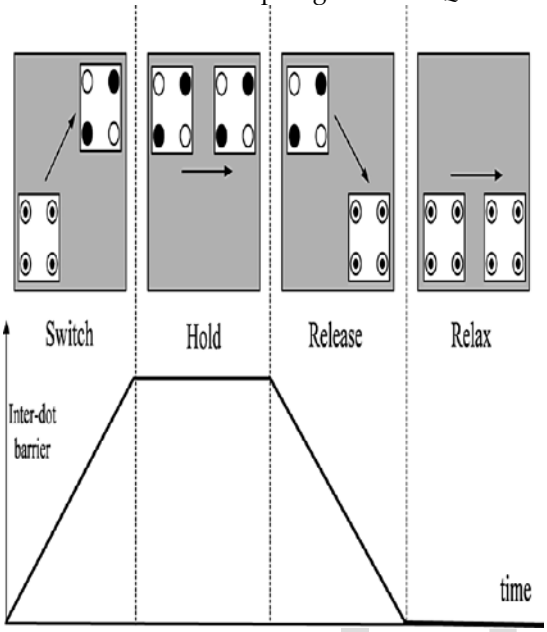

Fig.10 Four phases of a QCA clock.

retain their states. In the Release phase, the barriers are lowered and the cells are allowed to relax to an unpolarized state. Finally, in the Relax phase, the barriers are kept low and the cells remain unpolarized. A QCA circuit is partitioned into serial zones. These zones can be of irregular shape, but their size must be within certain limits imposed by fabrication and dissipation concerns. All cells in the same zone are controlled by the common clock signal. The scheme of clock zones permits an array of QCA cells to make a certain calculation and then have its state frozen, and finally, have its output serve as the input to the next clock zone.

5 REVERSIBLE FLIP-FLOP

The D flip flop is a modification of the clocked RS flip flop. In the D flip flop, the D input goes directly to the S input and its complement is applied as an R input. The D flip flop designed from irreversible gates. The D flip flop designed from the reversible equivalent gates.

The proposed circuit of the flip flop is evaluated in terms of number of reversible gates used and garbage outputs produced.

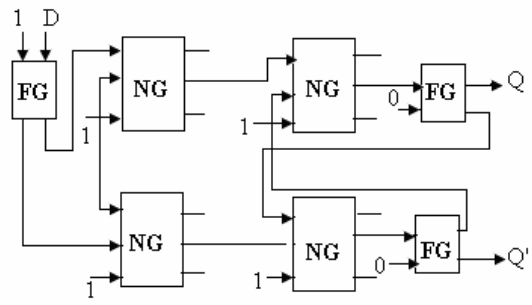

Fig.11 Reversible D Flip Flop

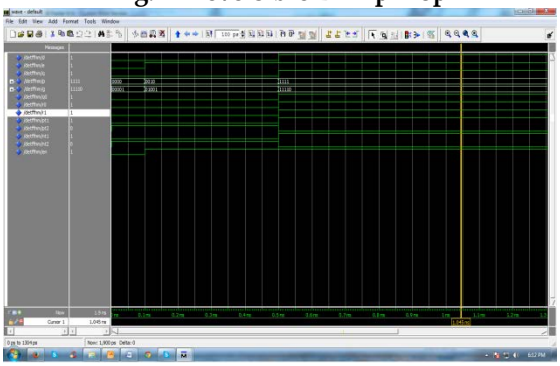

Fig.12 Output for reversible D Flip Flop

s

6 TESTING APPROACH TO QCA COMPUTING

QCA computing provides a promising technology to implement reversible logic gates. The QCA design of Fredkin gate using the four-phase clocking scheme in which the clocking zone is shown by the number next to D (D0 means clock 0 zone, D1 means clock 1 zone, and so on). It can be seen that the Fredkin gate has two level MV implementation, and it requires 6 MVs and four clocking zones for implementation. The number of clocking zones in a QCA circuit represents the delay of the circuit (delay between the inputs and the outputs). Higher the number of clocking zones, lower the operating speed of the circuit. In QCA manufacturing, defects can occur during the synthesis and deposition phases, although defects are most likely to take place during the deposition phase. Researchers have shown that QCA cells are more susceptible to missing and additional QCA cell defects. The additional cell defect is because of the deposition of an additional cell on the substrate. The missing cell defect is due to the missing of a particular cell. Researchers have been addressing the design and test of QCA circuits assuming the single missing/additional cell defect model.

7 CONCLUSION

Therefore conservative reversible logic gates are used to designed sequential circuits. The proposed system is used in the Feynman gate. This paper proposed reversible sequential circuits based on conservative logic that is testable for any unidirectional stuck-at faults using only two test vectors, all 0s and all 1s. The proposed sequential circuits based on conservative logic gates outperform the sequential circuit implemented

in classical gates in terms of testability. The sequential circuits implemented using conventional classic gates do not provide inherited support for testability. Hence, a conventional sequential circuit needs modification in the original circuitry to provide the testing capability. Also as the complexity of a sequential circuit increases the number of test vector required to test the sequential circuit also increases. For example, to test a complex sequential circuit thousand of test vectors are required to test all stuck-at-faults, while if the same sequential circuit is build using proposed reversible sequential building blocks it can be tested by only two test vectors, all 0s and all 1s. Thus, the main advantage of the proposed conservative reversible sequential circuits compared to the conventional sequential circuit is the need of only two test vectors to test any sequential circuit irrespective of its complexity. The reduction in number of test vectors minimizes the overhead of test time for a reversible sequential circuit. The proposed work has the limitation that it cannot detect multiple stuck-at-faults as well as multiple missing/additional cell defects. In conclusion, this paper advances the state-of-the-art by minimizing the number of test vectors needed to detect stuck-at-faults as well as single missing/additional cell defects.

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